Notice of Allowability	Application No.	Applicant(s)	
	09/836,065	NAKSRIKRAM ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *04/12/2005*.

2. ☒ The allowed claim(s) is/are *1-18*.

3. ☒ The drawings filed on *04 January 2005* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JOSEPH TORRES
PRIMARY EXAMINER

6/29/05

RD

DETAILED ACTION

Applicant's arguments presented in the Appeal Brief filed April 12, 2005 are fully considered and are persuasive. As a result, the finality of the previous action is withdrawn and a new/updated search in light of the arguments was performed and it is concluded that the claims of present application are in condition for allowance and below are the reasons.

REASONS FOR ALLOWANCE

Claims 1-18 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 1 of the present application teaches a method for testing a semiconductor device having a first sector of a first sector type memory size and a second sector type memory size, the method comprising: measuring a first time period related to a erasing the first sector; establishing a first test limit based on the first time period; measuring a second time period related to erasing the second sector; establishing a second test limit based on the second time period; and determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test. The foregoing limitations are not found in the prior arts of record. The prior art of record, namely Noguchi, teaches a method and apparatus for performing erase testing on a semiconductor device. Noguchi teaches a memory device in a bare chip state which is determined as fail by over erasing during a test at a wafer level, information indicating the presence of an over-erased memory cell is stored in a nonvolatile and readable manner into an identification memory circuit, and then memory cells in

a memory cell array are restored to an erase state of an electrically neutral state by irradiation with an energy beam such as ultraviolet rays. A chip erased by the energy beam such as ultraviolet rays is assembled as an OTPROM (one-time programmable read only memory) and tested. At that time, a writing/erasing control circuit for controlling data writing into and data erasing in the memory cells is brought into an operation-inhibited state in accordance with the information stored in the memory circuit. It is possible to reduce the rate at which fail products are produced by use of a flash memory which is determined as fail because of the presence of an over-erased memory cell as a one-time programmable memory device. Furthermore, Noguchi teaches (Figure 14) the erasing operation of a nonvolatile semiconductor memory device. First, at the stage of initializing, a program high voltage Vpp is applied to the instruction port controller 2 to render the instruction port controller 2 operative (a step S2). Then, specific data (00H) is programmed for all bytes (data input/output is carried out in the units of byte and erasing is carried out also in the units of byte) (a step S4). This data programming is made in order to bring each memory cell into a write state and set the threshold voltage of each memory cell to be substantially equal. In addition, each counter is preset to a predetermined initial value (a step S6). This counter includes a counter for counting the number of time CUMTEW of the increase of an erase pulse width TEW, and a counter for counting the number of times PLSCNT by which erase pulses are generated. An address is set to 0. Then, an erase setup instruction is written into the instruction port controller 2 (the status register 235 and the instruction register 237) (a step S8), and an erase instruction is subsequently written into the instruction port controller 2 (a step S10). An erasing with respect to all the memory cells is executed in accordance with the writing of the erase instruction (a step S12). After a predetermined time

period has passed, it is determined that the erasing of the memory cells is completed, and an erase verify instruction is written into the instruction port controller 2 (the status register 235 and the instruction register 237) (a step S14). In accordance with this erase verify instruction, an erase verify voltage is generated from the erase/program verification generator 9 and then transmitted via the X decoder 12 onto a selected word line in the memory cell array (a step S16). When a predetermined time period has passed (time T2), data reading is carried out (a step S18). If the read data is an erased data, then the data is "1". If the read data is an unerased data, then the data is "0". A determination is made as to whether this data is in the erased state or not in accordance with its value (a step S20). If the data indicates the unerased state, then an erase pulse width to be applied to erase the data is incremented by a predetermined value, and this incremented erase pulse width information is stored in the TEW counter (a step S22). A determination is first made as to whether the erase pulse width stored in the TEW counter reaches a maximum limit value, and subsequently, a determination is made as to whether the number by which the erase pulses are applied reaches a predetermined value (64 times) (a step S24). When the erase pulse application number PLSCNT reaches the predetermined value (64 times), it is determined that no erasing is allowed for that memory cell any more, and an erase error is stored (a step S26). When the erase pulse application number PLSCNT does not reach the predetermined value in the step S24, the processing returns to the step S8, in which the writing and erasing operation by the erase setup instruction and the erase instruction is carried out. None of the prior arts of record teach nor fairly suggest all the limitations in the independent claim 1 of the present application. In particular, the limitations of "...measuring a first time period related to a erasing the first sector; establishing a first test limit based on the first time

period; measuring a second time period related to erasing the second sector; establishing a second test limit based on the second time period; and determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test" are not taught nor fairly suggested in the prior arts of record.

Independent claim 10 include similar limitations of independent claim 1 and therefore is allowed for similar reasons.

Dependent claims 2-9 and 11-18 depend from independent claim 2 and inherently include limitations therein and therefore are allowed as well.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.

Mujtaba Chaudry
Art Unit 2133
June 29, 2005

JOSEPH TORRES
PRIMARY EXAMINER